PerfectVIPs
Right Tools... Perfect Chip

FIBRE CHANNEL VIP

GENIE-FC™

FC VERIFICATION IP

OVERVIEW

The Genie-FC™ Verification IP Products are the industry's most comprehensive verification solution for FC based designs. Its intelligent **Verification Engine**, integrated **Interface Inspector** and comprehensive **Compliance Suite** provide the perfect combination of tools to ensure first silicon success.

The **Genie-FC™ VIP** provides a quick and efficient way to verify any FC based design– Initiator, Switch or Target. It supports FC 1.1, 2 and 3 specifications and tests all layers of the FC protocol –FC-0, FC-1, FC-2, FC-3, & FC-4 . Genie-FC provides a complete verification solution that includes multi-language support and UVM, OVM and VMM methodologies.

The Genie-FC™ VIP provides:

- Initiator & Target Models
- Directed and Random Transaction Generator
- Frame & Primitive Generator
- Error Injector & Callbacks
- Monitor/Checker
- Report Generator
- Scoreboard
- Functional Coverage

Fig. 1: Point to Point topology

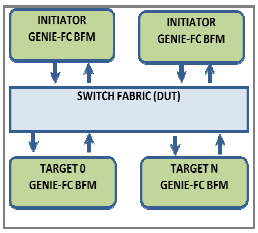

Fig. 2: Fabric topology

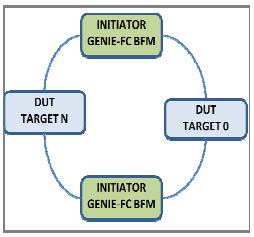

Fig. 3: Loop topology

FEATURES

❖ Initiator and Target models for complete FC Verification of Initiators, Targets and Switches	❖ Verifies all protocol layers (FC-0, FC-1, FC-2, and FC-4)
❖ Supports serial (1 bit) and parallel (10/16/20/32/40 bit) interface	❖ SAM-3/4 Application level exerciser for System level and block level testing
❖ Supports link speeds 1/2/4/8/10/16/20/32G with Speed Negotiations	❖ Supports 8b10b as well as 64b66b encoding & decoding
❖ 8 bit Encoder / Decoder interface, Dword level transport interface, Frame transaction level interface	❖ Automated FC Traffic generation in each layer ❖ Disparity & Kcode/Dcode Checking
❖ Protocol Checker – functionality at all layers	❖ Support for Configurable L, N, and F ports
❖ Scoreboard capability for data integrity checking	❖ Supports multiple instantiations in a test bench multi-port Initiators or Targets)
❖ Latest FC standards compliant	❖ Scalable for multiple instantiations in a testbench (multi-port Initiator/Target testing)
❖ Error Injections & ability to enable or disable specific error checks and violations	❖ Configurable test generation for constrained random, directed and error testing
❖ Programmable parameters through configurable Knobs	❖ Ability to control and change packet value during transmission through each layer
❖ User configurable reports for logging events and transactions	❖ Multiple Language Interface – SystemVerilog, Verilog, VHDL, C/C++, SystemC, 'e', VERA
❖ Automatic and user configurable Callback capability	❖ Packet corruption at bit level granularity
❖ Comprehensive Compliance Suite	❖ Supports OVM, UVM and VMM

UVM VMMenabled OVM

DATASHEET
Rev. 7

PRODUCT DETAILS

Initiator Model Features

Fibre Channel **Initiators Bus Functional Models** comes with a wide range of configurable attributes provides engineers with a flexible, scalable Model to simulate real world environments.

- Initiator capable of connecting to multiple Targets.
- Generates multiple FC Traffic data patterns including Random and User Defined
- Ability to Inject multiple Error conditions
- Sends specific or custom commands
- Capability to discover target information or skip discovery step and come up with appropriate target profile
- Performs Task Management functions
- Configurable login parameters and behavior

Target Model Features

Fibre Channel **Target Bus Functional Models** comes with a wide range of configurable attributes provides engineers with a flexible, scalable Model to simulate real world environments.

- Multiple error conditions and triggers allow for complex error injection.
- The ability to program complex and varying range of target configurations
- Supports block mode device
- Multiple LUN capability
- Responds to Fibre Channel traffic & specific or custom commands.
- Capable of responding to discovery commands such as INQUIRY, REPORT_LUNS, etc
- Supports several queuing attribute models
- Configurable LUN parameters
  - o Speed
  - o Size
  - o Personality
  - o Errors

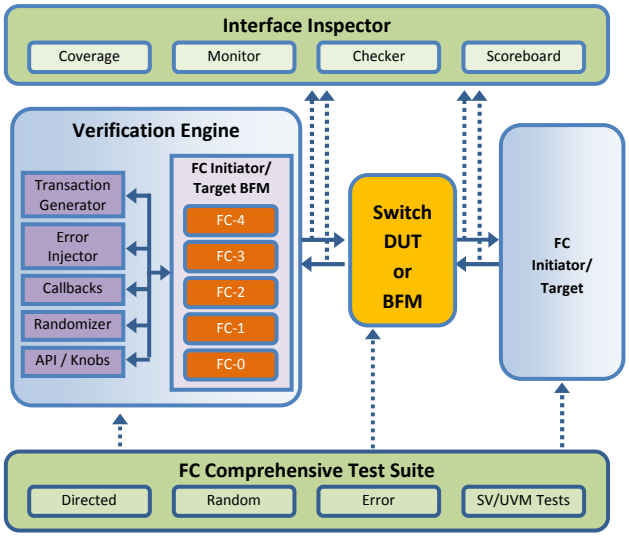

Fig 2: FC Verification Environment

Other Features

- Direct backdoor access to HDD memory
- Supports multi LUN addressing
- Frame Level error detection
- Supports CRC checking on received frames and optional CRC checking or insertion for transmitted frames.
- Buffer-to-buffer credit management support
- Statistics-gathering block for Frame Level, FCP Statistics & N port Statistics
- Speed-negotiation block
- Programmable parity checking of transmit data
- Support Port Login and Process Login
- Extended Link Services stimulus/response
- Supports multiple outstanding IOs/exchanges
- Ordered Set Sequence Validation
- Elasticity Buffer
- Controls for Dword/Primitive override
- FC Port State Machine & FC-AL2 State Machine
- Real time statistics and performance data

SUPPORTED SIMULATORS	ALDEC CADENCE MENTOR SYNOPSYS

FC COMPLIANCE SUITE	FC SOLUTIONS
Developed by PerfectVIPs to thoroughly exercise FC designs, the compliance suite is a comprehensive verification test suite that provides hundreds of test cases. ▪ Verifies all layers of FC designs ▪ Provides comprehensive design coverage targeted at FC-0,FC-1,FC-2,FC-3 & FC-4 layers ▪ Identifies all protocol violations ▪ Provides directed and constrained random regression testing capability ▪ Developed with actual customer designs	Developed by PerfectVIPs to address different system level FC architectures, the following FC solutions are available. Verification IP: ▪ FC Initiator VIP ▪ FC Target VIP ▪ FC Initiator/Target VIP Compliance Suites: ▪ Initiator Compliance Test Suite ▪ Target Compliance Test Suite

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